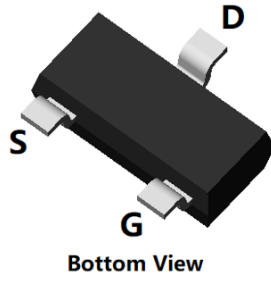
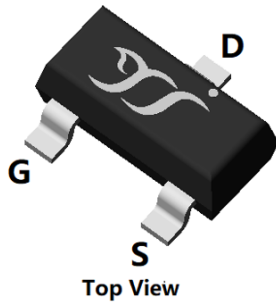
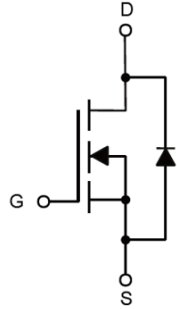


## N-Channel Enhancement Mode Field Effect Transistor



**SOT-23**



### Product Summary

• $V_{DS}$	100V
• $I_D$	2A
• $R_{DS(ON)}$ ( at $V_{GS}=10V$ )	<280mohm
• $R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	<310mohm

### General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- DC-DC Converters
- Power management functions

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	100	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ\text{C}$	$I_D$	2	A
	$T_A=70^\circ\text{C}$		1.6	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	8	A
Total Power Dissipation	$T_A=25^\circ\text{C}$	$P_D$	1.3	W
	$T_A=70^\circ\text{C}$		0.8	
Thermal Resistance Junction-to-Ambient <sup>B</sup>		$R_{\theta JA}$	96	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Case <sup>B</sup>		$R_{\theta JL}$	80	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL02N10A	F2	1002.	3000	30000	120000	7" reel



# YJL02N10A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	100			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS1</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
	I <sub>GSS2</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V			±50	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.1	1.8	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =2A		250	280	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =1A		260	310	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =2A, V <sub>GS</sub> =0V			1.2	V
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, f=1MHZ		387		pF
Output Capacitance	C <sub>oss</sub>			31		
Reverse Transfer Capacitance	C <sub>rss</sub>			28		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =2A		9.56		nC
Gate-Source Charge	Q <sub>gs</sub>			1.81		
Gate-Drain Charge	Q <sub>gd</sub>			1.97		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =2A, di/dt=100A/us		14.4		ns
Reverse Recovery Time	t <sub>rr</sub>			36.1		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =1.3A R <sub>GEN</sub> =1Ω		4		ns
Turn-on Rise Time	t <sub>r</sub>			17.8		
Turn-off Delay Time	t <sub>D(off)</sub>			13.2		
Turn-off fall Time	t <sub>f</sub>			28		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



## ■ Typical Performance Characteristics

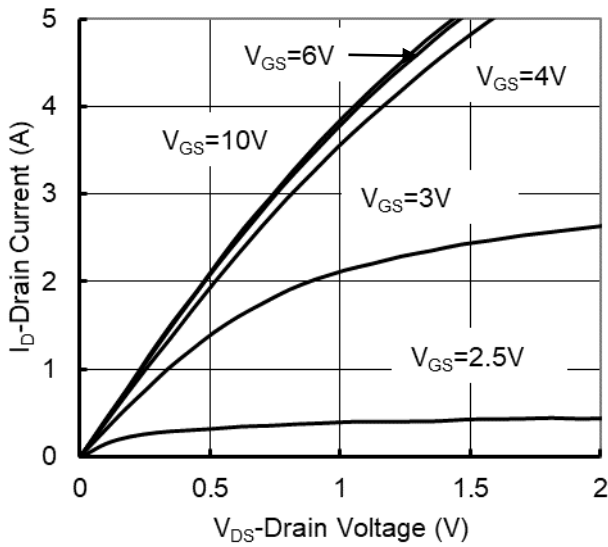


Figure1. Output Characteristics

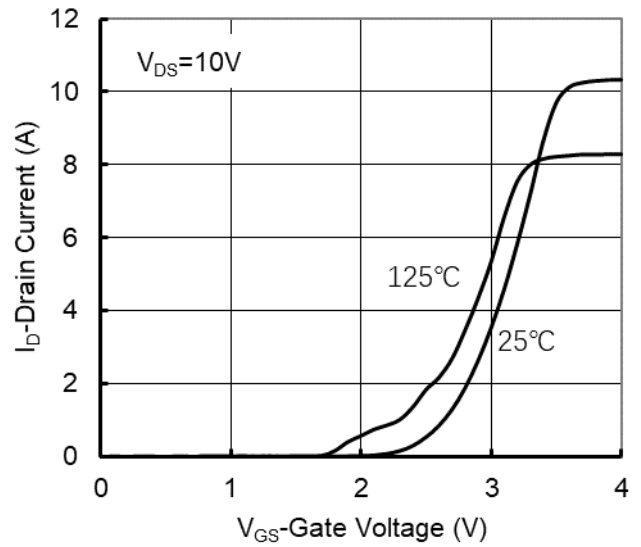


Figure2. Transfer Characteristics

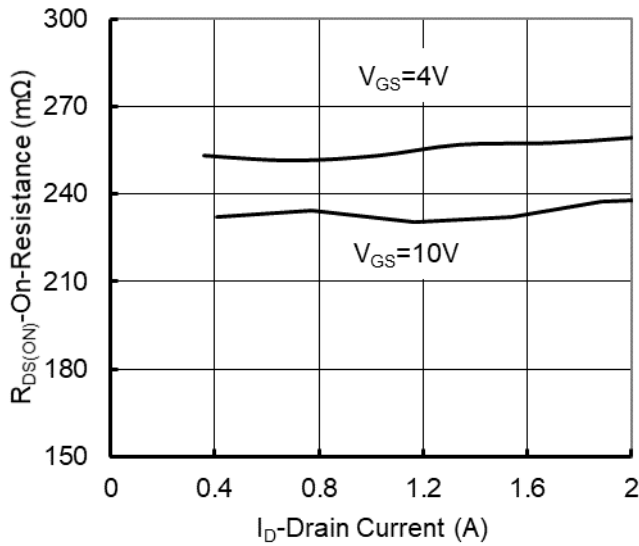


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

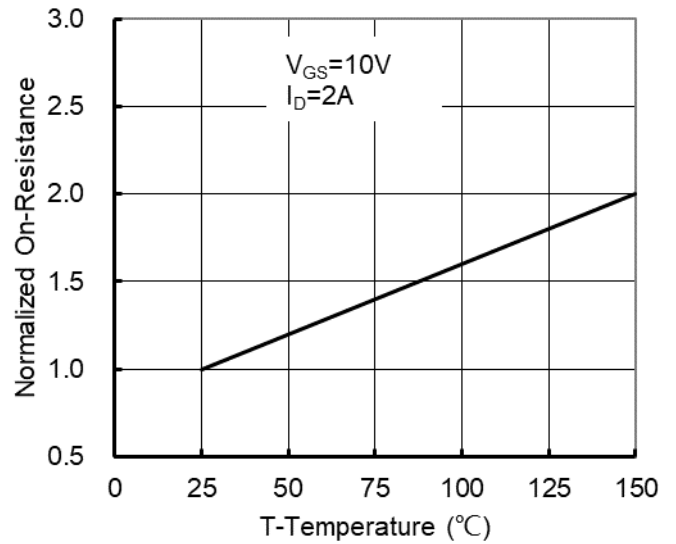


Figure 4: On-Resistance vs. Junction Temperature

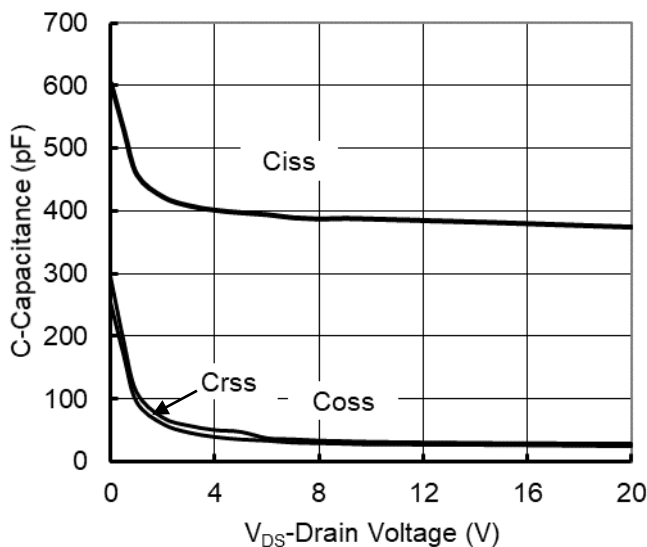


Figure5. Capacitance Characteristics

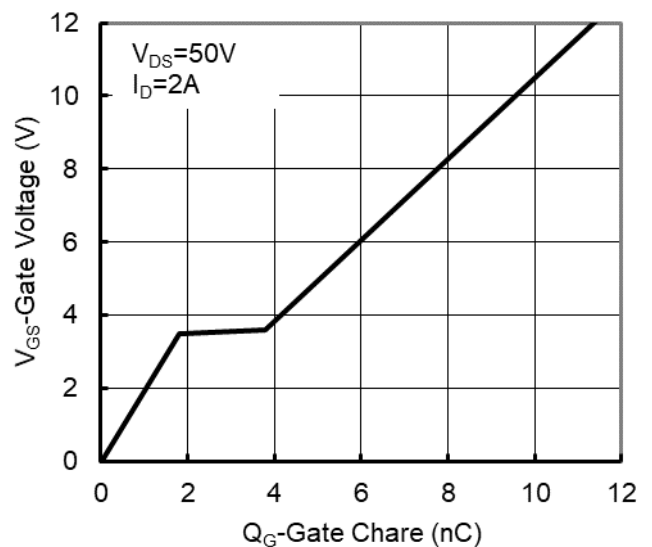


Figure6. Gate Charge



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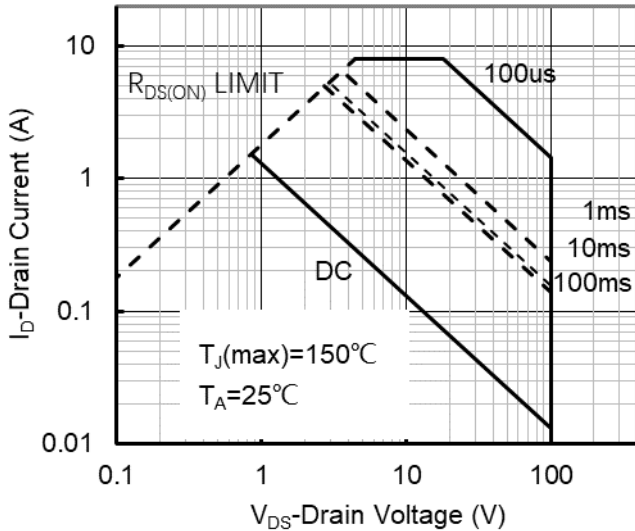


Figure7. Safe Operation Area

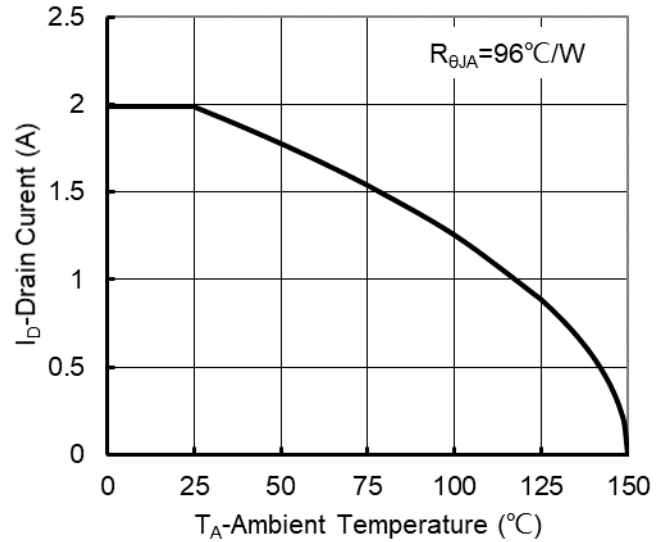


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

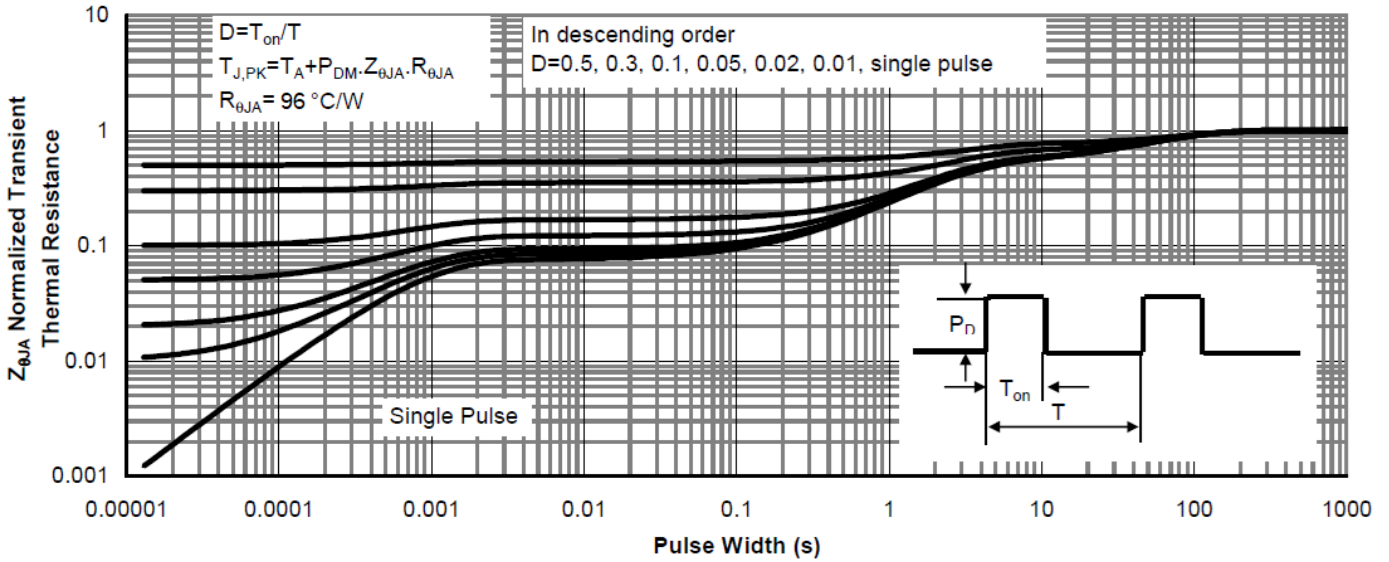
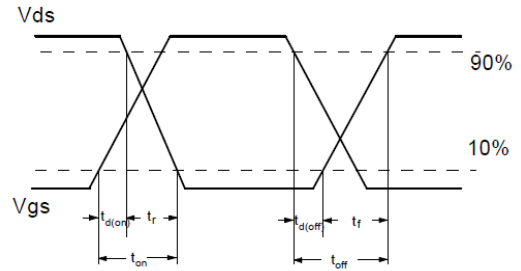
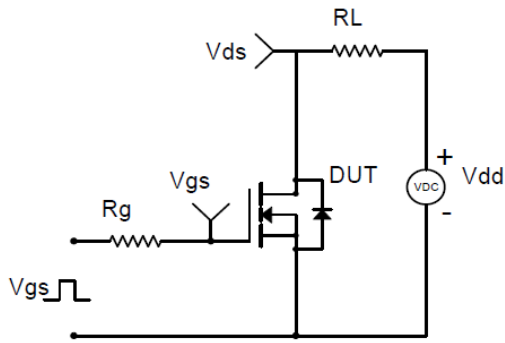
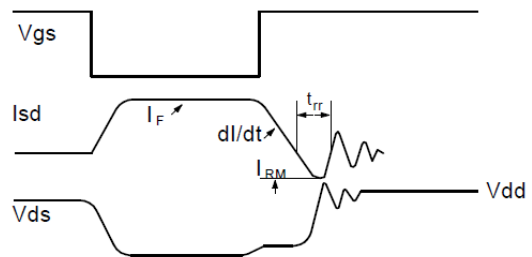
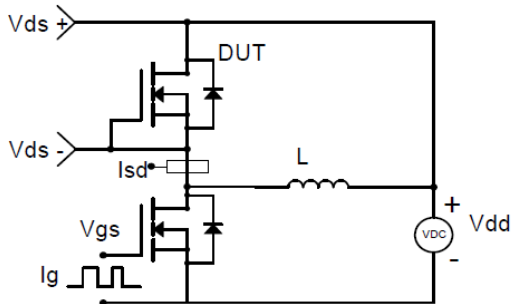


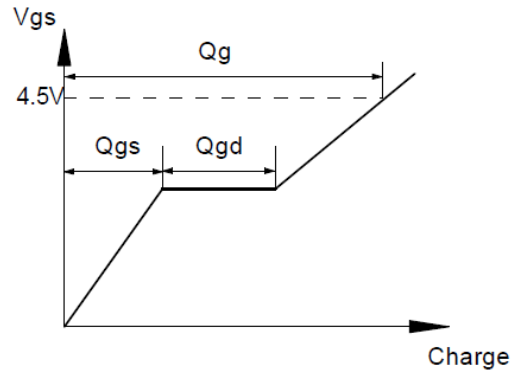
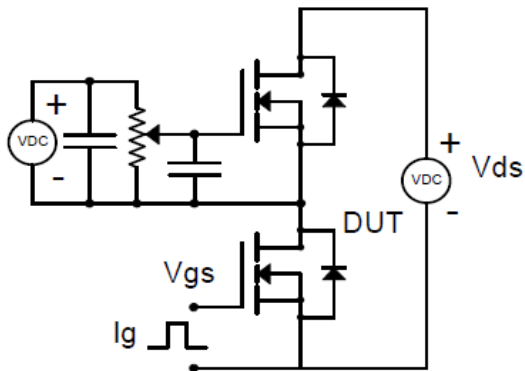
Figure9. Normalized Maximum Transient Thermal Impedance



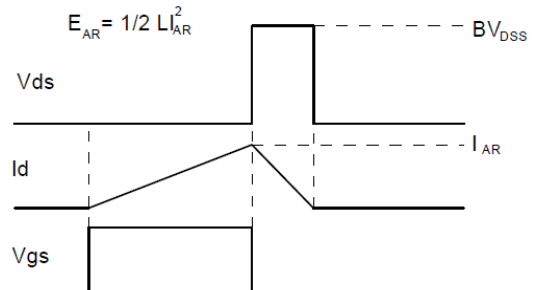
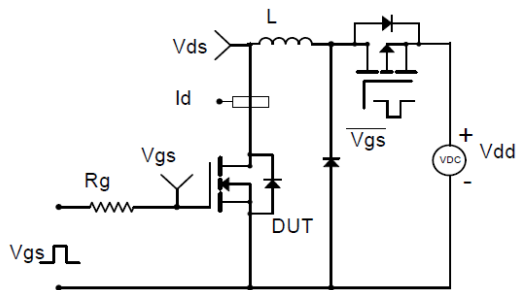
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

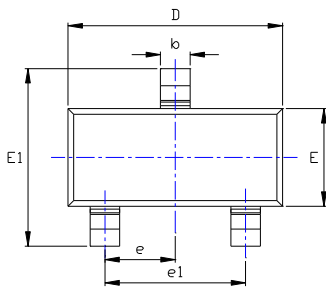


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

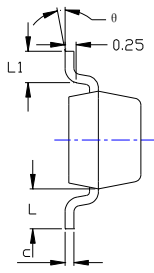


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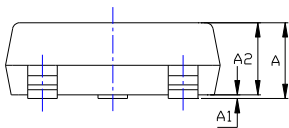
## ■ SOT-23 Package information



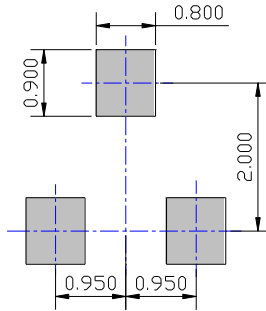
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

**NOTE:**

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



## YJL02N10A

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