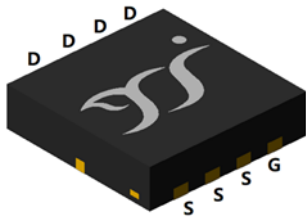
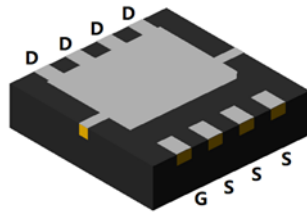


## P-Channel Enhancement Mode Field Effect Transistor

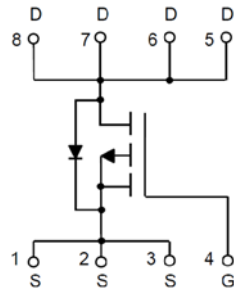


Top View



Bottom View

**DFN3333-8L**



### Product Summary

- $V_{DS}$  -60 V
- $I_D$  -30 A
- $R_{DS(ON)}$  (at  $V_{GS}=-10V$ ) <24m $\Omega$
- $R_{DS(ON)}$  (at  $V_{GS}=-4.5V$ ) <33m $\Omega$
- 100% EAS Tested

### General Description

- Trench Power LV MOSFET technology
- Low  $R_{DS(on)}$  & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Power management
- Portable equipment

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	-60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	-6	A
	$T_A=100^\circ C$		-3.5	
	$T_C=25^\circ C$		-30	
	$T_C=100^\circ C$		-19	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	-120	A
Avalanche energy <sup>B</sup>		EAS	100	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	2	W
	$T_A=100^\circ C$		0.8	
	$T_C=25^\circ C$		69	
	$T_C=100^\circ C$		27	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	$R_{\theta JA}$	50	60	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.4	1.8	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ30P06AJ	F1	Q30P06AJ	5000	10000	100000	13" reel



# YJQ30P06AJ

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V	-	-	-1	μA
		V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	-100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.0	-2.0	-3.0	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A	-	18	24	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-10A	-	24	33	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-20A, V <sub>GS</sub> =0V	-	-0.9	-1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz	-	5.0	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	-30	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, f=1MHz	-	4300	-	pF
Output Capacitance	C <sub>oss</sub>		-	170	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	150	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-30V, I <sub>D</sub> =-15A	-	61	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	17	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	7	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-15A, di/dt=100A/us	-	38	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	29	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DD</sub> =-30V, I <sub>D</sub> =-15A R <sub>GEN</sub> =4.5Ω	-	62	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	79	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	376	-	
Turn-off fall Time	t <sub>f</sub>		-	161	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=-40V, V<sub>G</sub>=-10V, L=0.5mH, I<sub>AS</sub>=-20A.

C. P<sub>d</sub> is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with T<sub>A</sub> =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



# YJQ30P06AJ

## Typical Electrical and Thermal Characteristics Diagrams

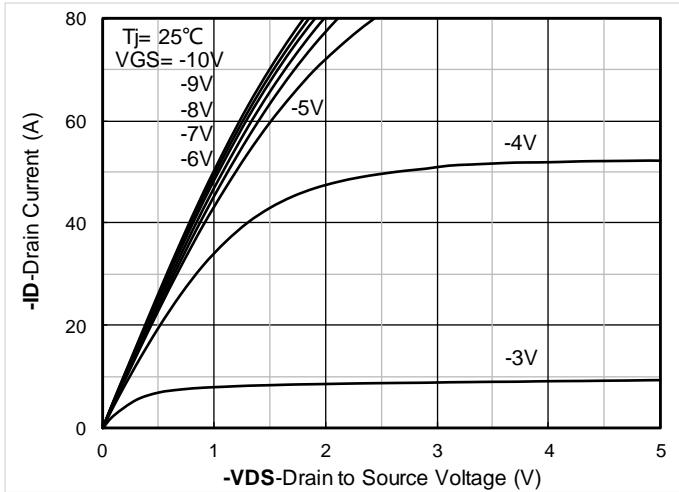


Figure 1. Output Characteristics

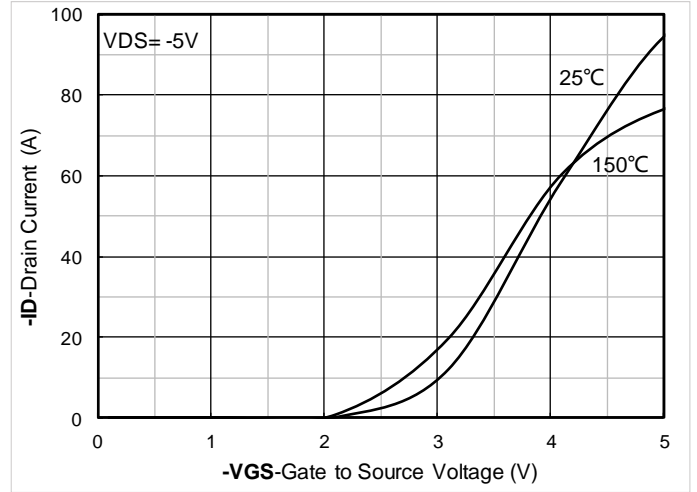


Figure 2. Transfer Characteristics

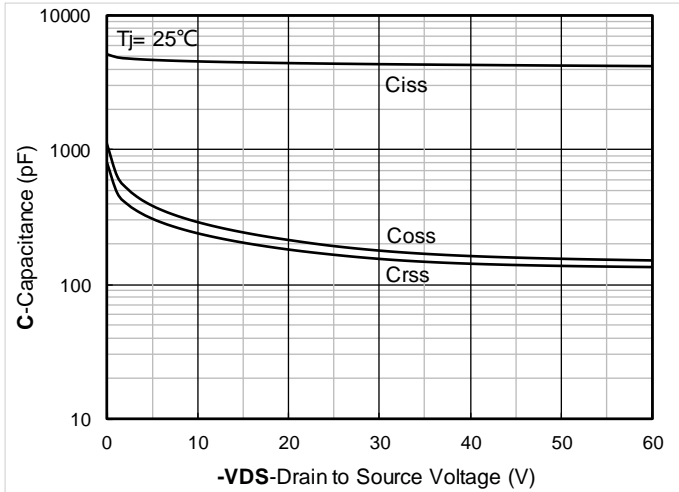


Figure 3. Capacitance Characteristics

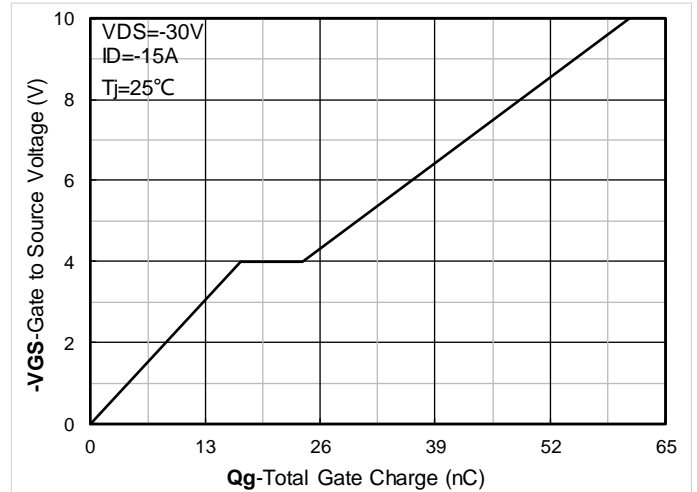


Figure 4. Gate Charge

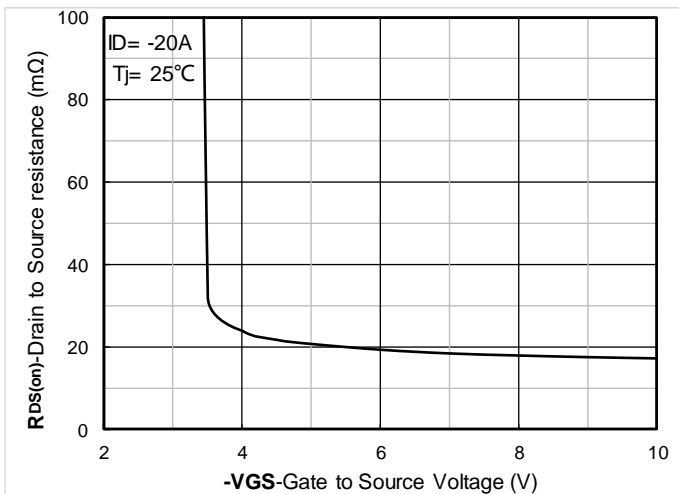


Figure 5. On-Resistance vs Gate to Source Voltage

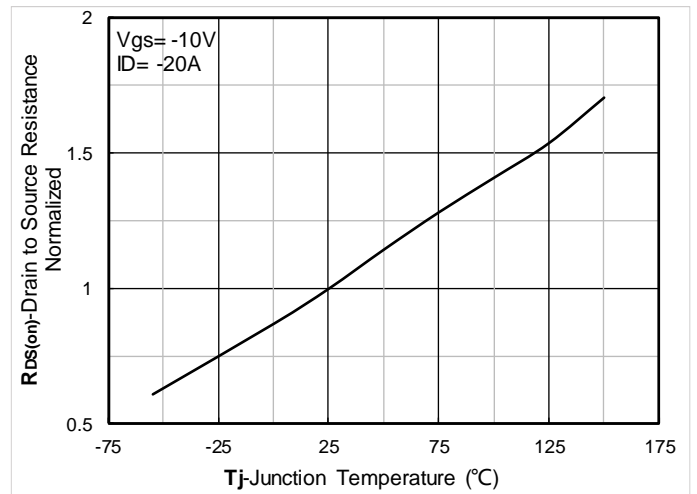


Figure 6. Normalized On-Resistance



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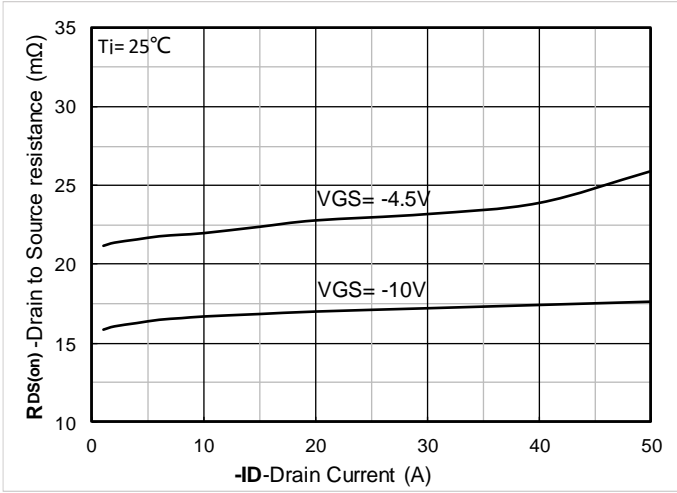


Figure 7.  $R_{DS(on)}$  VS Drain Current

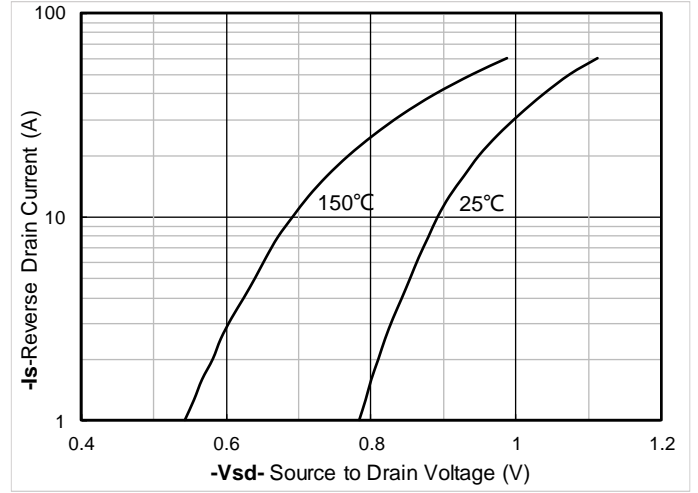


Figure 8. Forward characteristics of reverse diode

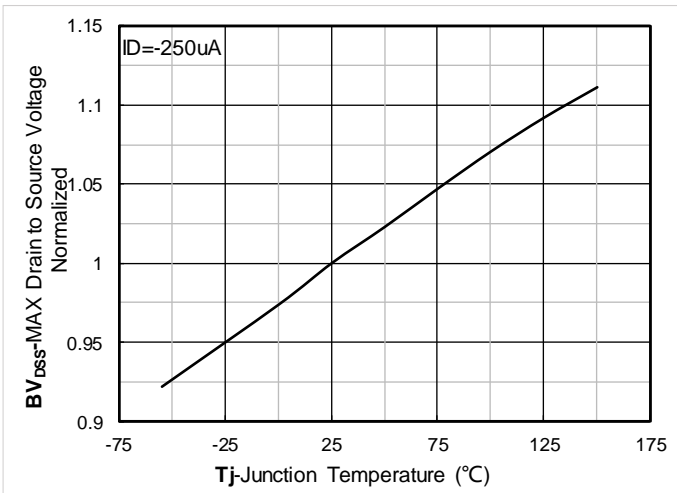


Figure 9. Normalized breakdown voltage

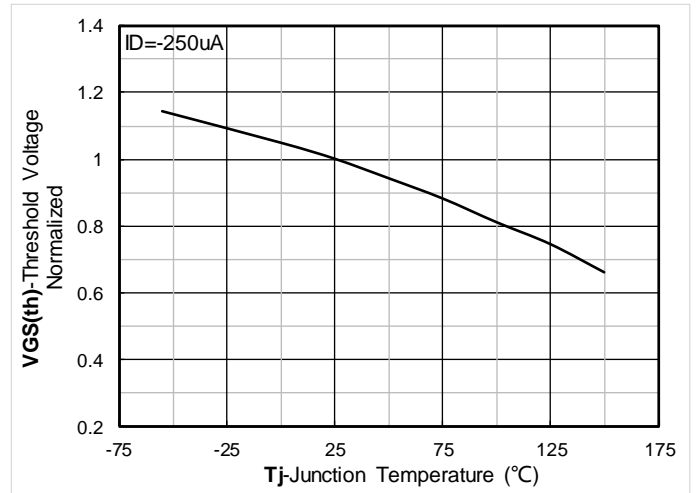


Figure 10. Normalized Threshold voltage

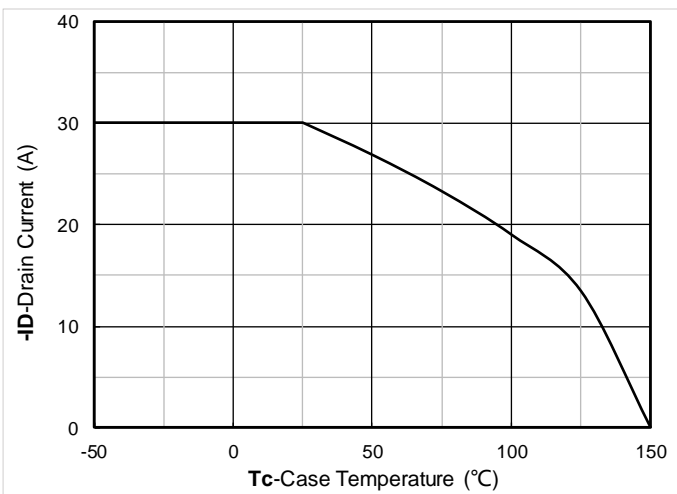


Figure 11. Current dissipation

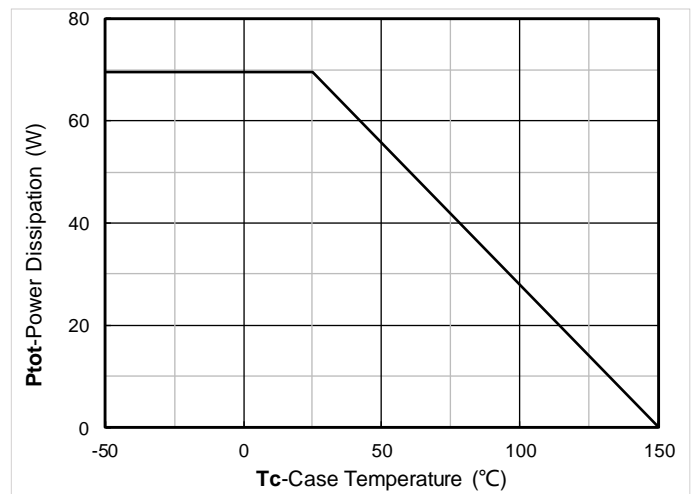


Figure 12. Power dissipation



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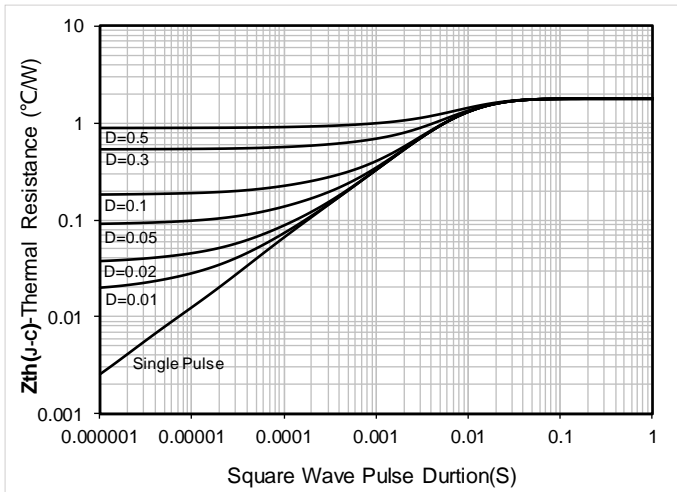


Figure 13. Maximum Transient Thermal Impedance

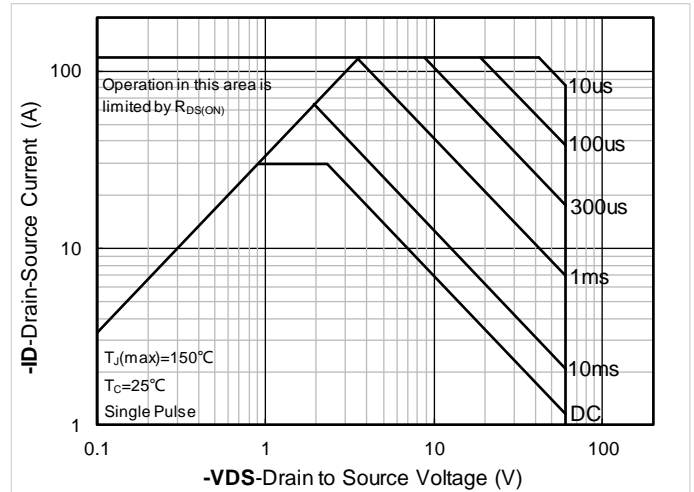
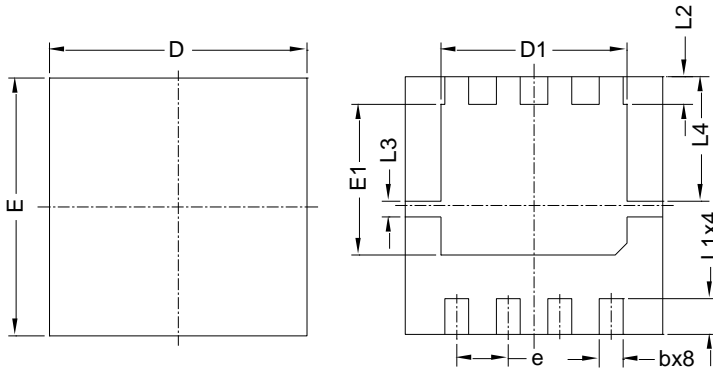


Figure 14. Safe Operation Area



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## DFN3333-8L Package information



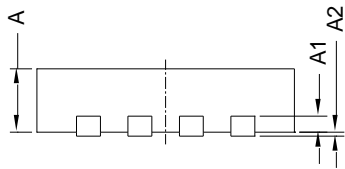
Top View  
正面视图

Bottom View  
背面视图

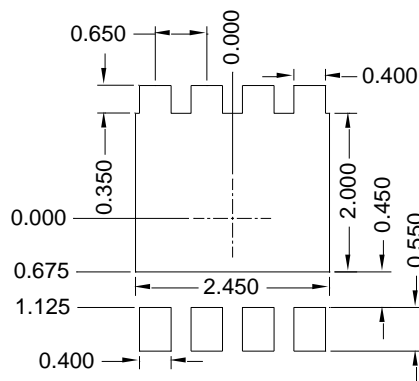
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
L3	0.20 BSC		
L4	1.57 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



Side View  
侧面视图



Suggested Solder Pad Layout  
Top View



## YJQ30P06AJ

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